Extending a MIPS Simulator for FPGA Support

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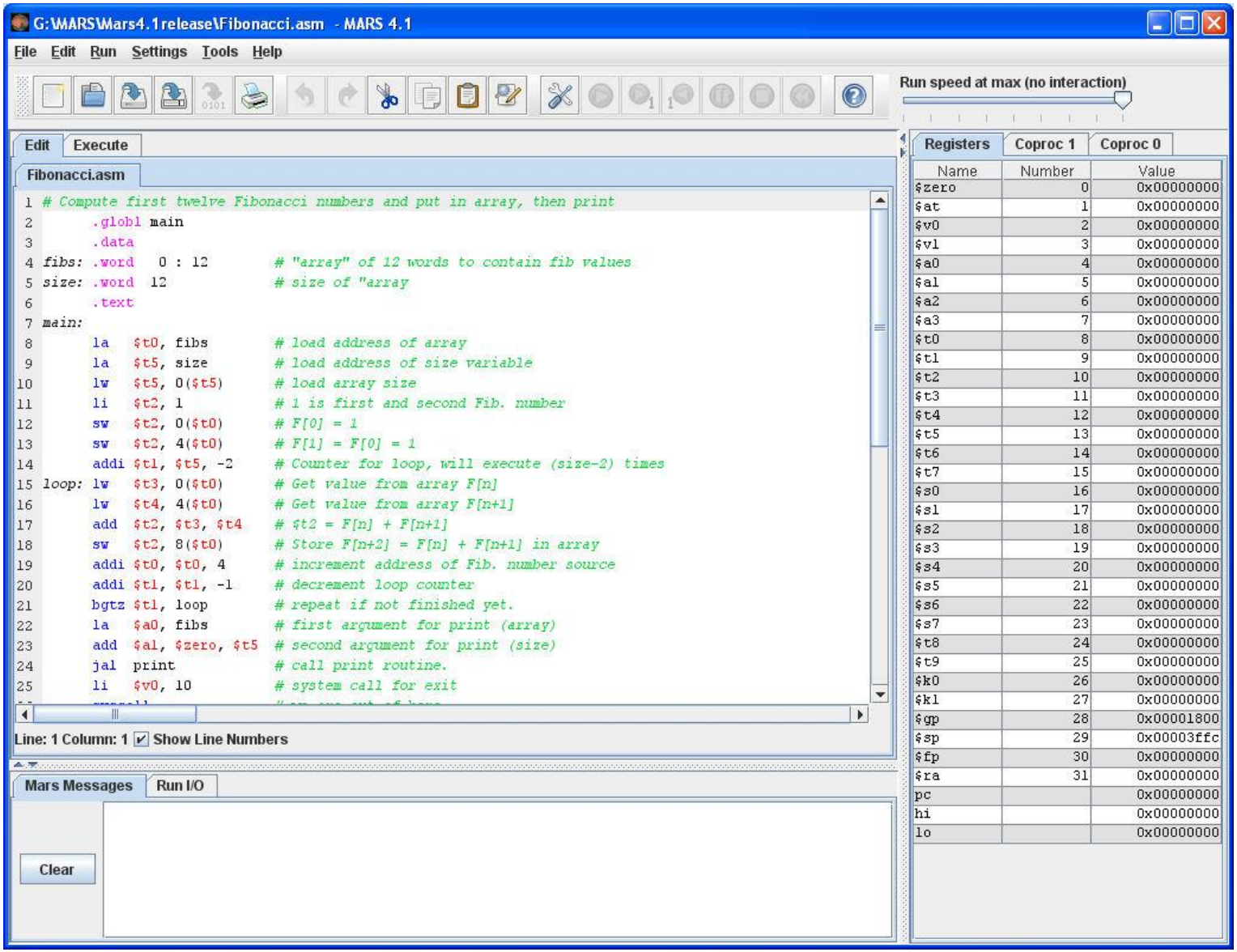
FPGA overview

- Field Programmable Gate Array (FPGA) is “programmable hardware.”
- Uses “hardware simulation” to execute a circuit design
- Design a circuit using components:
  - gates,
  - “mega-functions” (e.g., ALU),
  - Intellectual property (IP)
  - VHDL or Verilog hardware design language
- Available in a range of capacity, cost, and environment
- Very attractive in an educational environment: flexible, re-usable, low cost.

MARS Overview

- **M**IPS **A**ssembler and **R**untime **S**imulator
- An IDE for MIPS assembly language programming
- Designed for use with *Computer Organization and Design* by Patterson & Hennessy
- First release in 2005. Two releases per year.
- Extended to support FPGA
  - Configurable memory model
  - Export memory contents to text file
- JAR download www.cs.missouristate.edu/MARS



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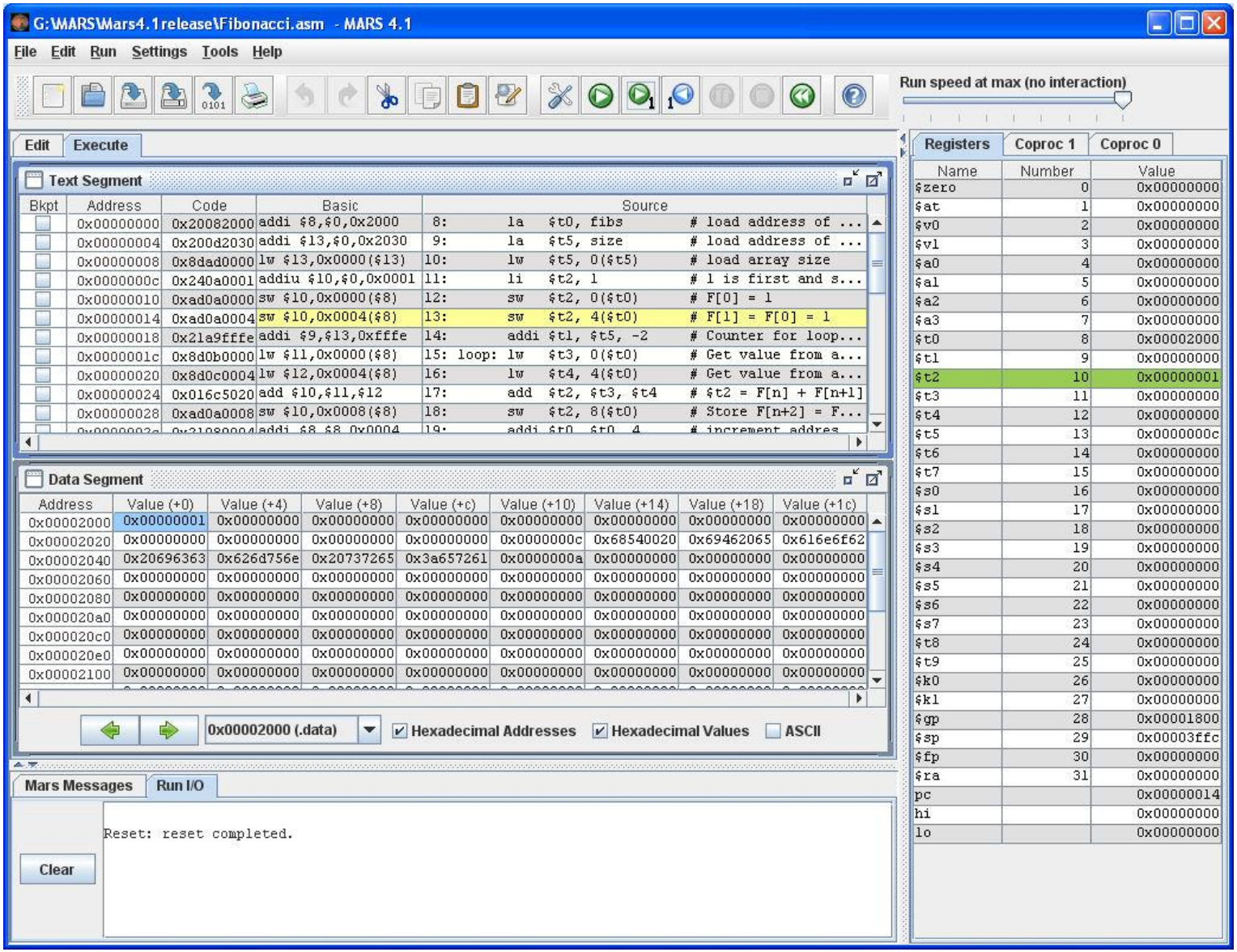

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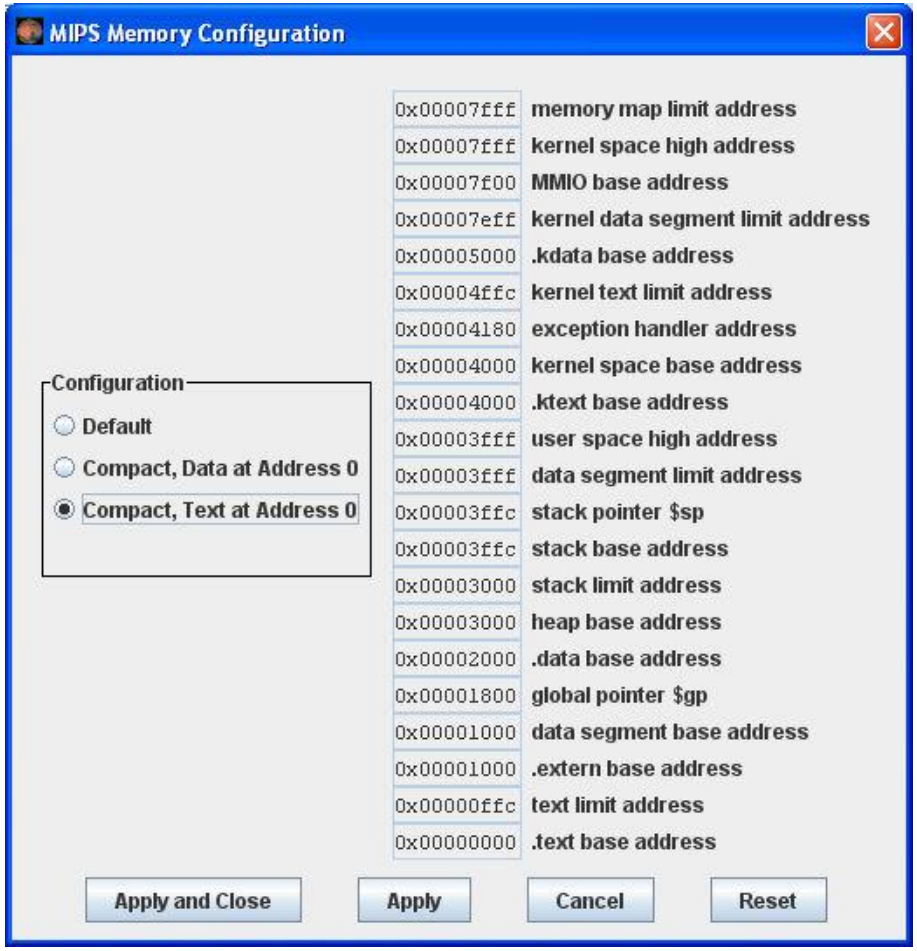
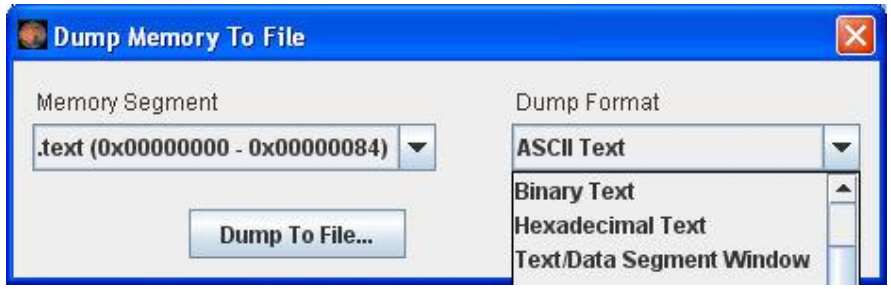
MARS features for FPGA support





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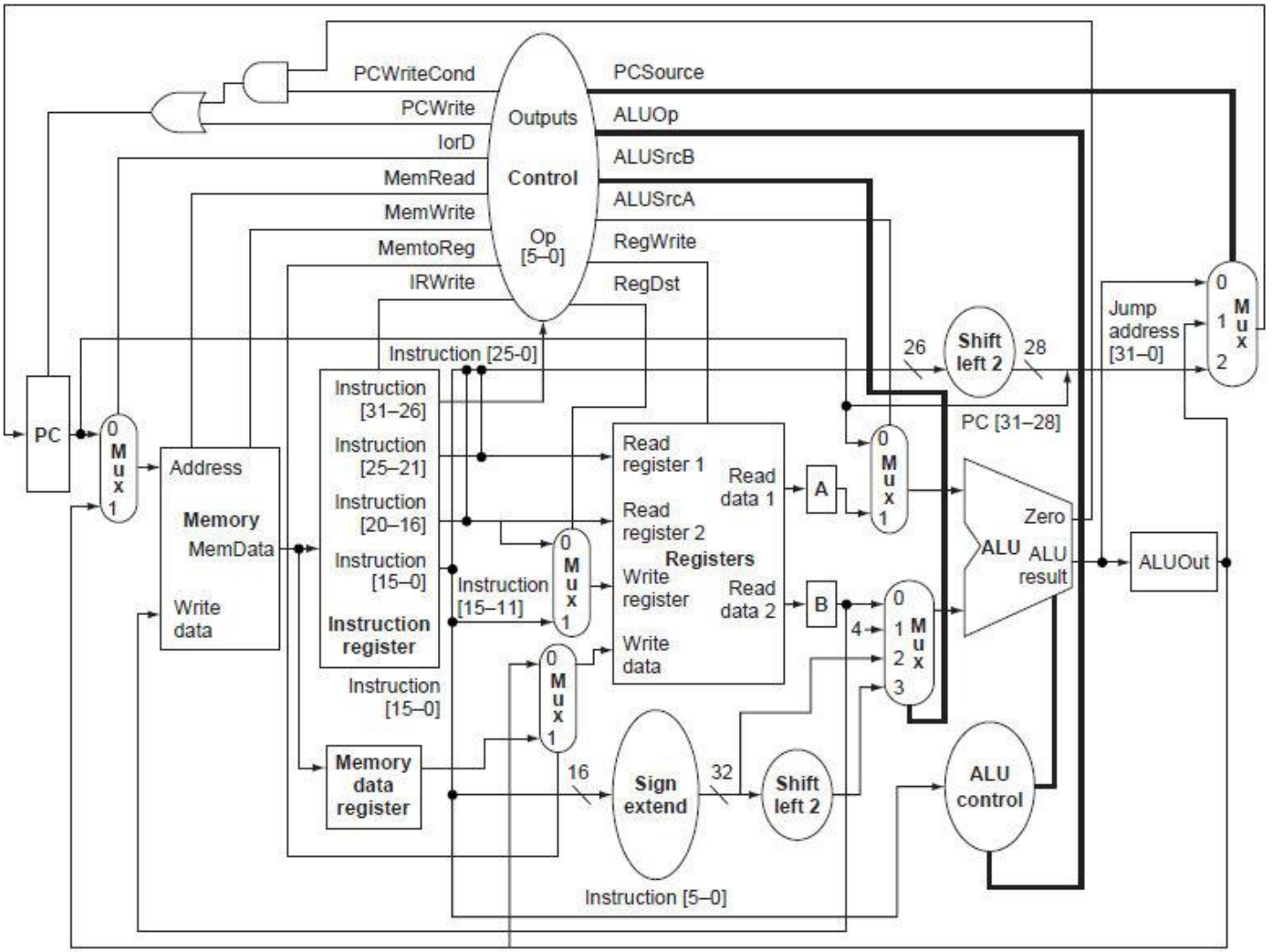
MIPS circuit design alternatives

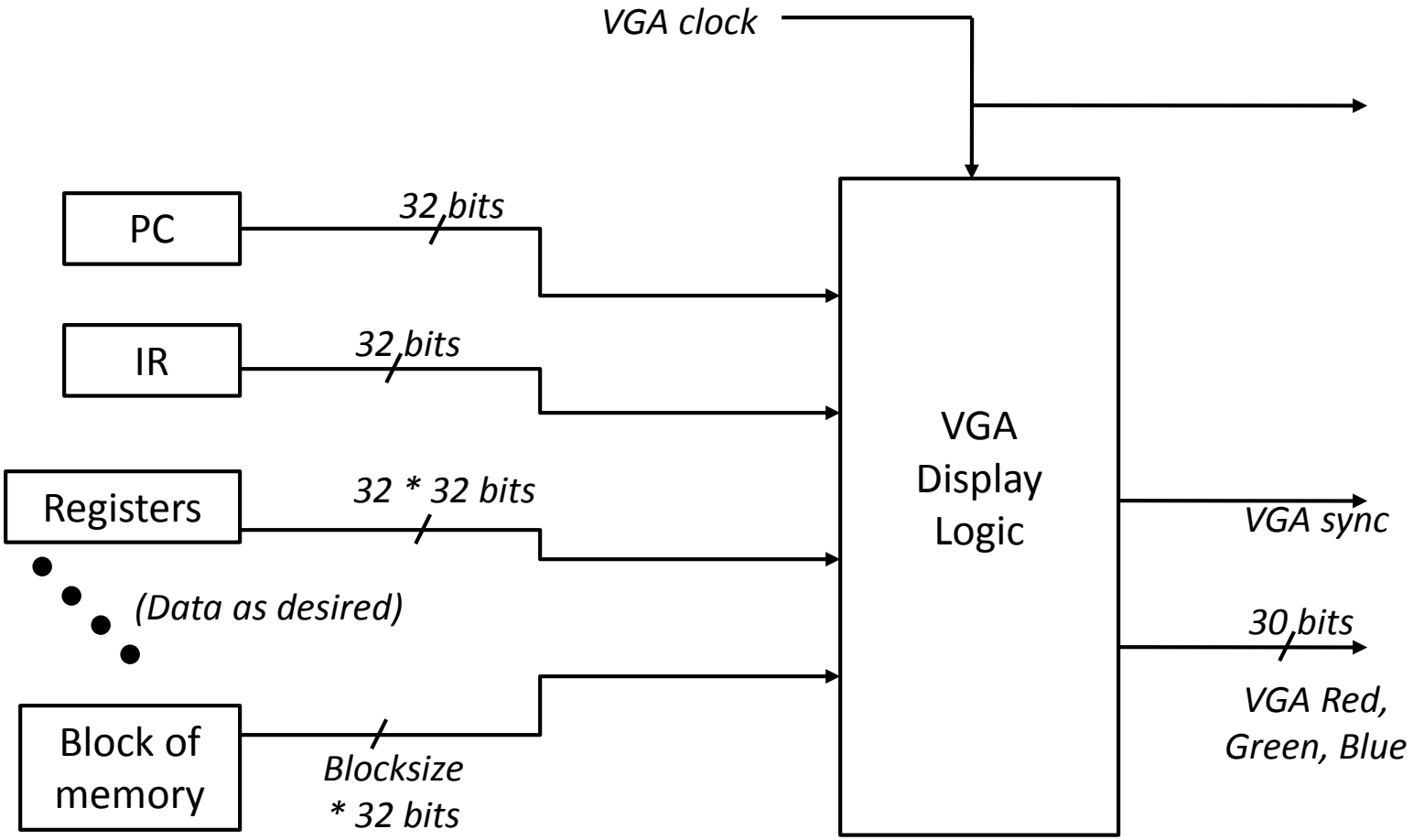
- Single-cycle
- Multi-cycle
- Pipelined

Two different circuits necessary

- MIPS circuit and the VGA display of the MIPS state
- Issue of “MIPS clock speed” vs. “VGA clock speed”
- MIPS memory not implemented in the FPGA itself, inefficient use of FPGA hardware simulation resources
- Instead, MIPS memory is contained in a separate RAM on the FPGA board
- This involves separate “memory load” steps for the MIPS memory and the MIPS circuit



Computer Organization and Design, 3rd Edition, Figure 5-28.


VGA clock
PC
32 bits
IR
32 bits
Registers
32 * 32 bits
(Data as desired)
Block of memory
Blocksize * 32 bits
VGA Display Logic
VGA sync
30 bits
VGA Red, Green, Blue

Usage in an architecture class

- Reinforce the concept of MIPS execution on various platforms:
  - A genuine MIPS processor
  - The MARS simulator of MIPS execution (running in Java on some other processor)
  - FPGA simulation of a MIPS processor (running with variable clock speed)
- Use spec sheets and manufacturer's data to estimate run times of different FPGA and MIPS implementations
- Add instructions to the MIPS implementation on FPGA

Acknowledgements

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Questions?