

Otterbein University

Digital Commons @ Otterbein

Mathematics Faculty Scholarship

Mathematical Sciences

2011

Extending a MIPS Simulator for FPGA Support

Pete Sanderson

Otterbein University, PSanderson@otterbein.edu

Follow this and additional works at: https://digitalcommons.otterbein.edu/math_fac



Part of the [Computer Sciences Commons](#), and the [Mathematics Commons](#)

Repository Citation

Sanderson, Pete, "Extending a MIPS Simulator for FPGA Support" (2011). *Mathematics Faculty Scholarship*. 6.

https://digitalcommons.otterbein.edu/math_fac/6

This Presentation is brought to you for free and open access by the Mathematical Sciences at Digital Commons @ Otterbein. It has been accepted for inclusion in Mathematics Faculty Scholarship by an authorized administrator of Digital Commons @ Otterbein. For more information, please contact digitalcommons07@otterbein.edu.

SIGCSE Special Project Showcase

Peter Sanderson
Otterbein University
Westerville, OH 43081
psanderson@otterbein.edu

2. EXTENDING A MIPS SIMULATOR FOR FPGA SUPPORT

This project enriches computer organization education by providing another avenue for execution of MIPS code. The initial and existing avenue is the MARS simulator for MIPS code, a well-established open source product for educational environments, in use at universities and colleges worldwide (<http://www.cs.missouristate.edu/MARS>). The new avenue is a special adaptation of MIPS circuitry on a Field Programmable Gate Array (FPGA) platform. FPGAs such as the Altera DE2 are very attractive in an educational environment because of their flexibility, re-use, and low cost. The FPGA MIPS circuit includes VGA graphical output for real-time display of the MIPS machine state, including registers, memory, etc. Students write MIPS code and compare its behavior and performance in the two environments of the MARS simulator and the FPGA MIPS hardware.