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Extending a MIPS Simulator for FPGA Support

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2. EXTENDING A MIPS SIMULATOR FOR FPGA SUPPORT

This project enriches computer organization education by providing another avenue for execution of MIPS code. The initial and existing avenue is the MARS simulator for MIPS code, a well-established open source product for educational environments, in use at universities and colleges worldwide (http://www.cs.missouristate.edu/MARS). The new avenue is a special adaptation of MIPS circuitry on a Field Programmable Gate Array (FPGA) platform. FPGAs such as the Altera DE2 are very attractive in an educational environment because of their flexibility, re-use, and low cost. The FPGA MIPS circuit includes VGA graphical output for real-time display of the MIPS machine state, including registers, memory, etc. Students write MIPS code and compare its behavior and performance in the two environments of the MARS simulator and the FPGA MIPS hardware.